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WHAT IS CLAIMED IS:

1. A semiconductor device, which comprises a semiconductor chip having a circuit-formed surface provided with a group of terminals thereon; a wiring layer having a wiring for connecting the group of terminals to a group of external terminals provided on the surface of the insulating layer, the surface facing the circuit-formed surface of the semiconductor chip; a three-layered buffer layer provided between the circuit-formed surface of the semiconductor chip and the wiring layer, the buffer layer comprising a structure having interconnected foams, an adhesive layer provided on the semiconductor chip-facing side of the structure having interconnected foams, directed to bonding to the semiconductor chip and another adhesive layer provided on the other side of the structure, directed to bonding to the wiring layer; a sealant for sealing connections of the group of terminal provided on the semiconductor chip to the wiring layer; and the group of external terminals connected to the wiring layer.

2. A semiconductor device according to Claim 1, wherein the buffer layer is a laminate obtained by pasting the two adhesive layers on both sides of the structure having interconnected foams, respectively.

3. A semiconductor device according to Claim 1, wherein the buffer layer is a laminate obtained by pasting the adhesive layers filled with an adhesive into pores of an interconnected foam structure on both sides

of the structure having the interconnected foams, respectively.

4. A semiconductor device according to Claim 1, wherein the structure having interconnected foams in the buffer layer is a porous body having a three-dimensional reticular structure.

5. A semiconductor device according to Claim 1, wherein the structure having interconnected foams in the buffer layer is a non-woven fabric of three-dimensionally entangled fibers.

6. A semiconductor device according to Claim 1, wherein the structure having interconnected foams in the buffer layer is composed of fluorine-containing resin.

7. A semiconductor device according to Claim 1, wherein the adhesive layers in the buffer layer are composed of thermosetting resin.

8. A semiconductor device according to Claim 1, wherein the adhesive layers in the buffer layer are composed of thermoplastic resin.

9. A semiconductor device according to Claim 1, wherein the group of terminals provided on the surface of the semiconductor chip are arranged in one direction on the central region on the circuit-formed surface of the semiconductor chip.

10. A semiconductor device according to Claim 1, wherein the set of terminals provided on the surface of the semiconductor chip are arranged in the peripheral

region on the circuit-formed surface of the semiconductor chip.

11. A semiconductor device according to Claim 1, wherein the wiring layer is provided with a window at a position of connection to the group of terminals on the semiconductor chip.

12. A semiconductor device according to Claim 1, wherein extensions of the wiring in the wiring layer are connected to the group of terminals provided on the semiconductor chip.

13. A semiconductor device according to Claim 1, wherein a semiconductor support substrate is provided on the surface opposite to the circuit-formed surface of the semiconductor chip.

14. A semiconductor device according to Claim 1, wherein a thickness ratio of the structure having interconnected foams to total buffer layer is at least 0.2.

15. A semiconductor device according to Claim 1, wherein the group of external terminals are arranged within the region of the semiconductor chip.

16. A semiconductor device, which comprises a semiconductor chip having a circuit-formed surface provide with a group of terminals thereon; a support substrate covering an opposite surface of the semiconductor chip to the circuit-formed surface and side ends of the semiconductor chip; a wiring layer comprising an insulating layer and a wiring for connecting the

group of terminals to a group of external terminals provided on the surface of the insulating layer, the wiring layer being provided on the side facing the circuit-formed surface of the semiconductor chip and extended over to the support substrate; a three-layered buffer layer provided between both of the circuit-formed surface of the semiconductor chip and the support substrate and the wiring layer, the buffer layer comprising a structure having interconnected foams, an adhesive layer provided on the semiconductor chip-facing side of the structure having interconnected foams, directed to bonding to the semiconductor chip and another adhesive layer provided on the other side of the structure, directed to bonding to the wiring layer; a sealant for sealing connections of the group of terminals provided on the semiconductor chip to the wiring layer; and the group of external terminals connected to the wiring layer, positioned on the support substrate.

17. A semiconductor device, which comprises a semiconductor chip having a circuit-formed surface provided with a group of terminals thereon; a support substrate covering an opposite surface of the semiconductor chip to the circuit-formed surface and side ends of the semiconductor chip; a wiring layer comprising an insulating layer and a wiring for connecting the group of terminals to a group of external terminals provided on the surface of the insulating layer, the wiring layer provided on the side facing the circuit-formed surface

of the semiconductor chip and extended over to the support substrate; a three-layered buffer layer provided between both of the circuit-formed surface of the semiconductor chip and the support substrate and the wiring layer, the buffer layer comprising a structure having interconnected foams, an adhesive layer provided on the semiconductor chip-facing side of the structure having interconnected foams, directed to bonding to the semiconductor chip and another adhesive layer provided on the other side of the structure, directed to bonding to the wiring layer; a sealant for sealing connections of the group of terminals provided on the semiconductor chip to the wiring layer; and the group of external terminals connected to the wiring layer, positioned within the region of the semiconductor chip and on the support substrate.

18. A semiconductor device according to Claim 16, wherein the group of terminals on the semiconductor chip are arranged in the peripheral region of the circuit-formed surface of the semiconductor chip.

19. A semiconductor device according to Claim 17, wherein the group of terminals on the semiconductor chip is arranged in the peripheral region of the circuit-formed surface of the semiconductor chip.

20. A wiring tape for a semiconductor device, which comprises a wiring layer comprising an insulating layer and a wiring on the insulating layer, one end of the wiring being connected to terminals on the

semiconductor chip and the other end of the wiring being connected to external terminals for connecting to a package substrate; and a three-layered buffer layer bonded to the wiring-formed side of the wiring layer, the buffer layer comprising a structure having interconnected foams, an adhesive layer provided on the semiconductor chip-facing side of the structure having interconnected foams, directed to bonding to the semiconductor chip and another adhesive layer provided on the other side of the structure, directed to bonding to the wiring layer.

21. An adhesive tape according to Claim 20, wherein a thickness ratio of the structure having interconnected foams to total buffer layer is at least 0.2.

22. An adhesive tape according to Claim 20, wherein the buffer layer is composed of a laminate prepared by pasting both sides of the structure having interconnected foams with the adhesive layers, respectively.

23. A wiring tape according to Claim 20, wherein the buffer layer is composed of a laminate prepared by pasting both sides of the structure having interconnected foams with adhesive layers each comprising a structure having interconnected foams whose pores are filled with an adhesive, respectively.